Local disorder effects in silicon nanodevices

H. Mizuta[1)], Y. Furuta[1)], G. Evans[2)], K. Nakazato[1)] and H. Ahmed[2)]

[1)]Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Madingley Road, Cambridge CB3 0HE, UK

[2)]Microelectronics Research Centre, University of Cambridge, Madingley Road, Cambridge CB3 0HE, UK

Heavily doped crystalline silicon (c-Si) and polycrystalline silicon (poly-Si) nanowires (NWs) have widely been used as a building block for Coulomb blockade (CB) memory and logic devices by utilising nanometer-scale electron islands naturally formed by local disorders. However, the microscopic properties of the electron islands and tunnel junctions have not been studied in detail, and there has been no clear guideline to optimise them. The aim of this work is to clarify and control the local disorder effects on electron transport in the silicon nanodevices.

In c-Si NW structures, local electrostatic potential disorder caused by randomly distributed ionised donors is responsible for natural formation of electron islands. For investigating this effect, we have performed a numerical simulation of the silicon NWs, in which random dopants are explicitly treated and the electron distribution is calculated self-consistently. A typical sample result of the electron distribution is shown in Fig. 1(a) for a 400-nm-long rectangular parallelepiped c-Si NW with a cross sectional area of 20 nm x 10 nm and donor concentration of 10^{20} cm^{-3}. A linear chain of electron islands is formed in the c-Si NW, resulting in a quasi-one-dimensional (1D) multiple tunnel junctions (MTJs). The current-voltage characteristics for the c-Si NW have then been calculated by feeding the capacitance and tunnel resistance parameters obtained for these electron islands into the Monte Carlo single-electron simulator. The offset charge effect in the c-Si NW has also been investigated by generating random fractional offset charge q_{offset} onto these electron islands repeatedly. Figure 1(b) shows the distribution of threshold voltage V_{th} obtained for the c-Si NW shown in Fig. 1(a). It was found that the average V_{th} becomes about 10 mV larger than the original V_{th} that we obtained for the c-Si NW without any offset charge. This offset-charge-induced V_{th} enhancement is caused by charge pinning phenomenon that occurs particularly in 1D MTJ systems.

On the other hand, in the poly-Si NW structures, individual silicon grains and grain boundaries (GBs) are supposed to act as an electron island and a tunnel junction, respectively. We have introduced poly-Si point contact transistor (PC-Tr) structure where both length and width of the NW channel are as small as the grain size, and the channel contains either zero or very few GBs (See Fig. 2(a)). Therefore, the electric characteristics for the PC-Trs are supposed to show properties of electron transport via an individual GB. First, we studied the PC-Trs fabricated by using an as-deposited poly-Si film. The PC-Trs exhibited either linear or non-linear I-V characteristic that are attributed to a channel without and with GBs, respectively. No CB effects were observed for any of fabricated devices. The temperature dependence of resistivity has been analysed by using a simple thermionic emission model, and the effective potential barrier height of GBs was found to range from 30 meV to 80 meV. In contrast clear CB oscillation has been observed for the oxidised PC-Trs as GBs are converted to sub-oxide layers, SiO_x with $x<<2$, in the oxidation process. The relationship between the GB tunnel barrier parameters and CB characteristics will be discussed in more detail by showing the results for PC-Trs prepared with various process conditions.

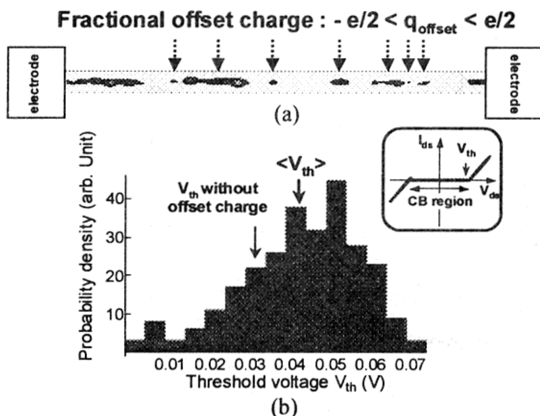

Fig.1 (a) Electron density distribution calculated for a c-Si NW structure with donor concentration of 10^{20} cm^{-3}. The areas with electron density less than $0.001Cm^{-2}$ are set to zero. (b) The distribution of threshold voltages obtained for the c-Si NW structure with random fractional offset charge introduced onto the electron islands.

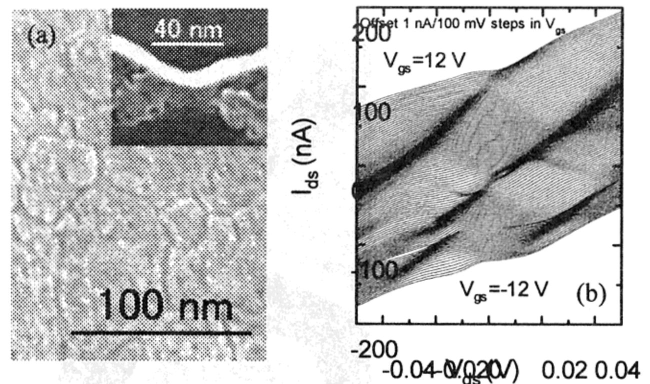

Fig. 2 (a) An SEM image of a secco etched poly-Si film. Grain size ranges from 20 nm to 150 nm. The inset figure shows ultra short NW channel of the unoxidised poly-Si PC-Tr structure. (b) Current-voltage characteristics observed for an oxidised poly-Si PC-Tr with varying side-gate bias at T = 9.0 K. Large rhombic-regions can be seen, corresponding to strong CB effects.