Room temperature single-electron devices in nanocrystalline silicon

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Nanocrystalline silicon material, consisting of silicon grains ~10 nm or less in size, raises the possibility of the fabrication of novel quantum and multifunctional silicon devices. We have fabricated nanometre-scale single-electron transistors operating at room temperature in 20 nm-thick nanocrystalline silicon thin films where the grain size is only 4 – 8 nm. The films were deposited at 300 °C using plasma-enhanced chemical vapour deposition, from a SiF_4 : H_2 : SiH_4 gas mixture, on a 150 nm-thick silicon dioxide layer grown thermally on an *n*-type crystalline silicon substrate. The crystalline volume fraction, determined using Raman spectroscopy, was 70%. The films were heavily-doped *in situ* using PH_3 and the carrier concentration was 1×10^{20} /cm^3. TEM inspection and Raman spectroscopy indicated that the crystalline silicon grains were 4 – 8 nm in size and encapsulated by amorphous silicon tissues.

Our single-electron transistors consisted of 20 nm × 20 nm point-contacts with in-plane side-gates (Fig. 1). The devices were defined using electron beam lithography and reactive-ion etching. There were only 2– 3 grains in the cross-section of the point-contact, forming charging islands isolated by amorphous silicon tunnel barriers at the grain boundaries. This device showed single-electron effects at temperatures only up to 60 K. The maximum operating temperature was limited not by the grain size, which was small enough for room temperature operation, but by a tunnel barrier only 40 meV high. The barrier height was determined using activation energy measurements. We improved the tunnel barrier height by selectively oxidising the amorphous silicon grain boundaries using an LSI compatible low-temperature (750 °C) oxidation and high-temperature annealing (1000 °C) process. This encapsulated the grains with silicon oxide tissues, creating energy barriers up to 170 meV high. Single-electron conductance oscillations were observed in the I_{DS}-V_{GS} characteristics even at 300 K (Fig. 2). The 'natural' formation of nano-scale charging islands and tunnel barriers in our films raises the possibility of single-electron LSI memory and logic systems.

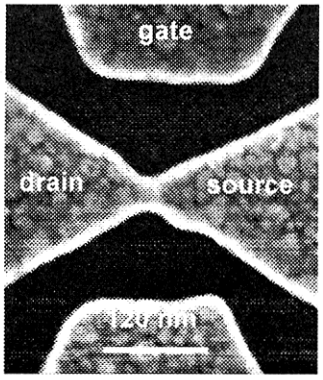

Figure 1

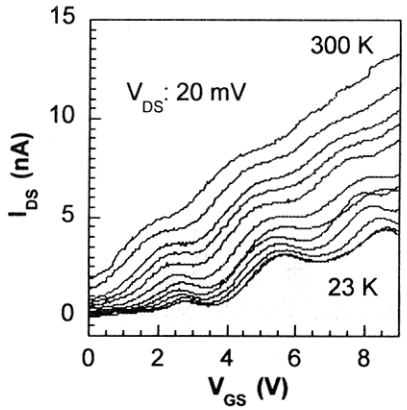

Figure 2