Ballistic transport devices using NeoSilicon

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Vertical transistor quantum point contact: Promising for future electron devices, the ballistic transport effect features no fluctuation and higher conductivity compared to the classical carrier transport. However, it has been hard to observe ballistic transport in Si devices due to a short mean free path. Presented here is a clear quantized conductance in Si due to ballistic transport measured at 5K using vertical transistor structures with a bias voltage of 1mV. The channel length is defined by the thickness of the CVD-grown Poly-Si gate electrode, 20nm. The channel width can be controlled by electric field confinement, using the wrap-around gate. Thus, it is easy to obtain a very small quantum point contact. Poly-Si channel, prepared by solid phase crystallization of CVD a-Si, is very high quality with a grain size of larger than 200nm and the electron mean free path of 40nm, confirmed by the Hall measurement. Moreover, the depletion layer between the channel and the gate oxide can reduce the interface scattering. These advantages enable the clear observation of the ballistic transport effect. On the other hand, the conductance at a higher bias voltage of 100mV was smaller than that at a low bias voltage and indicated no staircase-like characteristic. These characteristics indicate that the ballistic transport effect can increase the transconductance, which leads to a high reliability of a device operation at a low voltage supply, compared to the classical electron transport. By applying a magnetic field perpendicular to the channel, the conductance is reduced and splitted into many steps, which can be ascribed to spin and valley splitting. For a further investigation, we calculate theoretical conductance characteristics in an assumption of one-dimensional confinement. Si has six ellipsoidal valleys in k-space. This anisotropic characteristic in k-space makes a planar cross sectional shape of the channel and the direction of the electron transport sensitive to quantized sub-bands. The characteristics from non-ballistic transport, which is based on an ordinary J-FET, and ballistic transport, where the conductance is defined by quantized sub-bands, the device structure can be estimated. The theoretical curves, which are obtained by a calculation in an assumption of J-FET model and an effective mass approximation of the Schr dinger equation, can be fitted to experimentally observed curves. However, the calculated curve in magnetic fields, which is based on the Schr dinger equation including the magnetic vector potential equation for a consideration of spin and valley splitting, is quite different from the observed one. However, we can fit the curves to observed ones by taking into account the magnetic resistance of the Si channel connecting to the point contact caused by strong magnetic fields.

Cold electron emitters: A planar type cold electron emitter with narrow beam dispersion formed by porous Si (PS) has been proposed by Prof. Koshida. The feature includes high electron emission efficiency and simple fabrication processes. The dominant mechanism is that hot electrons ballistically transport through the PS layer and emit from the surface into vacuum. We can form Si quantum dots with well-controled nanometer sizes, in the plasma cell and deposit them onto any kind of substrates. This preparation method of nanocrystalline Si particles enables hybrid logic circuit including the electron emitter. The electron emitter is formed on an n^+-Si (0.01Ωcm) wafer as a electron source. The Si nanodots with diameters of 10±5 nm have been deposited on the substrate by 144MHz plasma decomposition of SiH_4. The surface of nano-Si dots are covered by naturally grown oxide. The shape of the dots are spherical and between dots there are many voids, which prevent an electric field effectively applied to the sample. To overcome this problem, we filled spaces with SiO_2 by melting SiO_2 surrounding Si dots using phosphorous diffusion. The impurities in SiO_2 reduce the melting point of SiO_2 because of the rearrangement of molecules in SiO_2. After the deposition of Si dots, the sample is annealed at 1100°C for 10minutes with P_2O_5, under nitrogen carrier gas. P atoms diffuse into Si dots and SiO_2 covering dots. SiO_2 including P atoms melts and fills into voids between dots. The thickness of Si layer with molten SiO_2 is 60nm. Finally a Au film is deposited onto the surface. Measurements are performed in vacuum with a back pressure of 10^{-6}torr. The Au electrode is grounded, and a metal plate as a collector of electrons extracted into a vacuum is located in front of the sample by the distance of 5mm and applied a constant positive voltage of 100V. While a negative voltage is applied to the Si substrate, a simple diode current is observed. When a negative voltage over 5V is applied, which corresponds to a work function of Au, electrons starte to be extracted from the sample and reach to the collector. At a voltage of −16V, an emission current and the emission efficiency, which is defined by the emission current to the total current, reached to 10μA/cm^2 and 4.8%, respectively. The mechanism is as follows; First, electrons are injected from the silicon wafer into nc-Si dots without scattering due to small size of dots. The electric field around dot is enhanced due to the spherical shape of dots. Thus the electrons from nc-Si are accelerated in SiO_2 by the high electric field, allowing ballistic transport through subsequent nc-Si layers. Electrons with a higher energy than the work function of Au are emitted from the surface to the collector. By optimizing the fabrication processes, we obtain the higher efficiency of 10% although the lifetime is short. Thus, this device promises the electron emitter with low power consumption.

Conclusion: Presented here are two devices taking advantage of ballistic transport in NeoSilicon, vertical transistors and electron emitters. High current drivability of ballistic transport region is clearly shown. High electron emission efficiency of 4.8% is obtained in planarized nanocrystalline silicon embedded in SiO_2.